THAT WHICH IS CLAIMED IS:

1. An integrated circuit chip, comprising:

a CAM-based search engine device that is configured to convert a learn portion of a search-and-learn (SNL) instruction associated with a search key into a search operation using the search key, in response to detecting a prior equivalent learn of the search key in said search engine device.

2. The chip of Claim 1, wherein a search portion of the SNL instruction and the search operation result in repeated searches of an internal database using equivalent comparands.

3. The chip of Claim 2, wherein a first one of the repeated searches generates a miss result; and wherein a second one of the repeated searches generates a hit result.

4. The chip of Claim 1, wherein said search engine device is further configured to prevent a pair of equivalent SNL instructions that result in immediately consecutive searches of an internal database from causing a duplicate learn event.

5. The chip of Claim 1, wherein said search engine device comprises a SNL cache memory device that is configured to store search keys that accompany SNL instructions and marker information that identifies whether the stored search keys are duplicates of other search keys within the SNL cache memory device.

6. The chip of Claim 5, wherein the SNL cache memory device operates as a first-in first-out (FIFO) memory device.

7. An integrated circuit chip, comprising:

a CAM-based search engine device that is configured to support conversion of a search-and-learn (SNL) instruction into a pair of equivalent search operations that are pipelined relative to each other when necessary to reduce the occurrence of duplicate learn operations within the search engine device.

8. The chip of Claim 7, wherein said search engine device comprises a SNL cache memory device that is configured to store search keys that accompany SNL instructions and marker information that identifies whether the stored search keys are duplicates of other search keys within the SNL cache memory device.

9. The chip of Claim 8, wherein the SNL cache memory device operates as a first-in first-out (FIFO) memory device.

10. An integrated circuit chip, comprising:

a CAM-based search engine device that utilizes a search and learn (SNL) cache memory device as a temporary search key buffer that supports operations to block the occurrence of duplicate learn operations within said search engine device.

11. The chip of Claim 10, wherein the SNL cache memory device operates as a first-in first-out (FIFO) memory device.

12. A method of operating a CAM-based search engine device, comprising the steps of:

searching a database within a CAM core with a search key to detect the presence of a hit or miss condition, in response to a search and learn (SNL) instruction; and

checking the search key to determine whether is has been marked as a duplicate, in response to detecting the presence of a miss condition.

13. The method of Claim 12, wherein said checking step is followed by the step of converting a learn portion of the SNL instruction into a search operation that results in another search of the database with the search key, in response to determining that the search key has been marked as a duplicate.

14. An integrated circuit chip, comprising:

a CAM-based search engine device that is configured to support internal conversion of a search-and-learn (SNL) instruction into a pair of search operations in order to prevent the SNL instruction from adding a duplicate entry into a database within said search engine device.

15. An integrated circuit chip, comprising:

a CAM-based search engine device that is configured to support processing of first and second immediately consecutive and equivalent search and learn (SNL) instructions as a first SNL instruction and a second search and search instruction, respectively, in order to block an addition of a duplicate learned entry into a database in said search engine device.

16. The chip of Claim 15, wherein said search engine device is further configured to selectively block processing of the second SNL instruction as a second search and search instruction in response to detecting the database as full when the first SNL instruction is processed.

17. The chip of Claim 16, wherein said search engine device comprises a cache memory device that operates as a temporary search key buffer that supports operations to process the second SNL instruction as a second search and search instruction in order to block the learning of at least one duplicate entry into the database.

18. The chip of Claim 17, wherein the SNL cache memory device operates as a first-in first-out (FIFO) memory device.

19. The chip of Claim 17, wherein the SNL cache memory device operates as content addressable memory device that is subject to aging operations.

20. An integrated circuit chip, comprising:

a CAM-based search engine device that utilizes a searchable cache memory device therein as a search key buffer that supports operations to block duplicate learn events from occurring within said search engine device.

21. The chip of Claim 20, wherein the cache memory device comprises a content addressable memory array.

22. The chip of Claim 21, wherein the content addressable memory array is configured to store search keys and database identification information.

23. An integrated circuit chip, comprising:

a CAM-based search engine device having a cache memory device therein, which is configured to retain search keys associated with previously processed learn instructions, and instruction execution logic therein that is configured to process a learn instruction and corresponding search key by searching the cache memory device to detect the presence of a duplicate search key before issuing the learn instruction to a CAM core within said search engine device.

24. The chip of Claim 23, wherein the cache memory device comprises a content addressable memory array.

25. A CAM-based search machine, comprising

a plurality of CAM-based search engine devices that are configured in a depth-cascaded arrangement and include at least one search engine device having a searchable cache memory device therein that is configured to store search keys and database identification information associated with learn instructions previously processed by the search machine and instruction execution logic that is configured to process a learn instruction and corresponding search key by searching the cache memory device to detect the presence of an equivalent search key before issuing the learn instruction to a CAM core in said plurality of CAM-based search engine devices.

26. The search machine of Claim 25, wherein the cache memory device comprises a content addressable memory array that is subject to aging.

27. The search machine of Claim 25, wherein the at least one search engine device is a master search engine device and the other search engine devices within said plurality of search engine devices are slave search engine devices.